8 S.E. / 4 Differential Analog inputs
4 High Current Analog Outputs
4 Individual Digital I/Os
for PCI Express Mini Card
Hardware Manual

Models **mPCIe-ADIOHC16-8FDS Family**

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MADE IN THE USA

Chapter 1: Quick Start

It is recommended that you install the software package before installing the PCI Express Mini (mPCIe) card in your computer. You can install the software[1] using our stand-alone installer downloaded from the website.

Run the installer you downloaded and follow the prompts to install the software for your device.

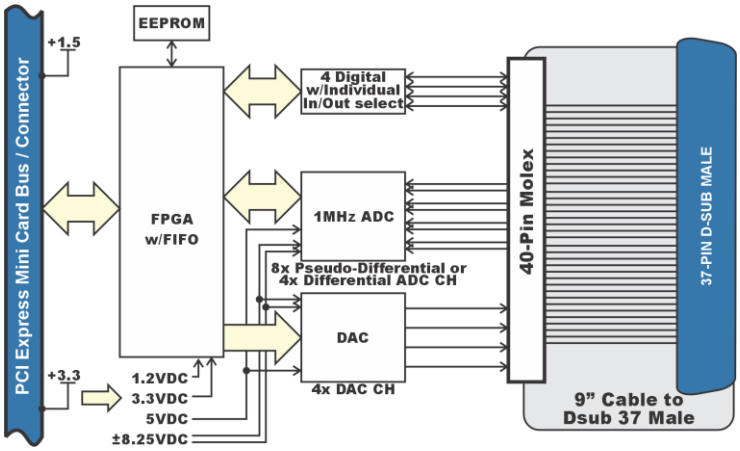
Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.

Once the software has been installed, shut down your system and carefully install the mPCIe card.

Re-start your system. Once the computer finishes booting, your new I/O should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the device displays a warning triangle, right-click and select "Update Driver".

[1] *In Linux or OSX please refer to* github.com/accesio/apci.

Chapter 2: Introduction



- PCI Express Mini Card (mPCIe) type F1 with latching I/O connector
- 16-bit, Bipolar, Differential, A/D converter
  - Software selectable as 8 Single-Ended (Pseudo-differential) or 4 Differential Inputs
  - Channel-by-channel programmable input ranges from ±0.3125V up to ±5V
  - Sustained sampling rates up to 1MHz
  - A/D starts via software, external input, or periodic timer
  - A/D "Scan Start" mode optimizes inter-channel timing
  - High impedance, 8-channel input: 500 MΩ
  - 32k FIFO plus DMA for efficient, robust data streaming
- Four 16-bit analog outputs @ ±2.5V, 0-5v, ±5V
  - Outputs Drive ±18mA Guaranteed
- 4× Digital I/O individually configurable for input/output
- Onboard Watchdog with status output
- RoHS compliant standard
- Optional Digital Integration Features: Pulse and PWM generation and measurement, edge-specific IRQs and counting.

Chapter 3: Hardware

This manual applies to the following models:		VEN:DEV
mPCIe-ADIOHC16-8FDS	A/D 16-bit, 1Msps, 4 Diff D/A w/ timed DAC Waveform playback	494F:C0C4
mPCIe-ADIOHC16-8F	A/D 16-bit, 1Msps, 4 Diff D/A	494F:C0C5
mPCIe-ADIOHC16-8A	A/D 16-bit, 500Ksps, 4 Diff D/A	494F:C0C6
mPCIe-ADIOHC16-8E	A/D 16-bit, 250Ksps, 4 Diff D/A	494F:C0C7
mPCIe-ADIOHC12-8A	A/D 12-bit, 500Ksps, 4 Diff D/A	494F:C053
mPCIe-ADIOHC12-8	A/D 12-bit, 250Ksps, 4 Diff D/A	494F:C054
mPCIe-ADIOHC12-8E	A/D 12-bit, 100Ksps, 4 Diff D/A	494F:C055

All models are full-length "F1" mPCIe devices, and RoHS compliant.

INCLUDED IN YOUR PACKAGE

1× mPCIe-ADIOHC16-8F Family card

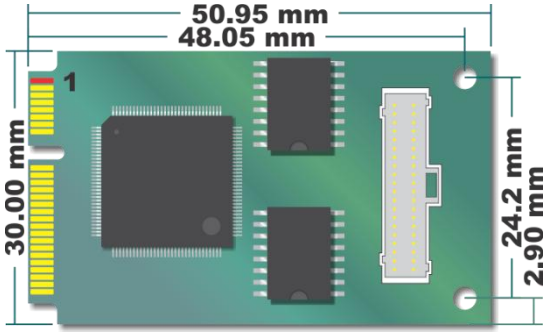
Available accessories include:	
CAB-mPCIe-ADIO	9 inch panel-mount DB37M twisted pair cable assembly
ADAP37F-MINI	Direct plug-on terminal board mates with DB37M on CAB-mPCIe-ADIO
LF-BRK-P9259-37	Mounting bracket for DB37M on CAB-mPCIe-ADIO
mPCIe-HDW-KIT2	Mounting hardware for 2mm mPCIe
mPCIe-HDW-KIT2.5	Mounting hardware for 2.5mm mPCIe

Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific application requirements, such as Industrial Temperature (-40°C to 85°C).

Chapter 4: Configuration Settings

All configuration of this device is performed through software; there are no jumpers or switches to set.

Chapter 5: PC Interface



This product interfaces with a PC using a PCI Express Mini Card (mPCIe) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

The small size and powerful performance, combined with perfect software compatibility with PCI and PCIe peripheral designs, have led to its recent adoption as a go-to standard for embedded Data Acquisition and Control, and many other applications.

Although mPCIe is a broadly-adopted industry standard, the actual connection to the computer shares a specification with mSATA:

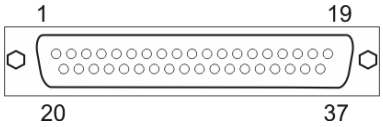
both mSATA and mPCIe use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either mPCIe or mSATA devices – and, according to the standards for mPCIe and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC documentation that your edge-connector is *actually* PCI Express Mini Card compliant before installing this, or any, mPCIe card. Damage might occur if you install an mPCIe device into a computer that only supports mSATA.

mPCIe defines mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose (which was a recurring problem with the older PCI Mini devices). Eliminating this concern for PCI Express Mini Cards is a major reason this standard has seen rapid adoption by the Data Acquisition and Control industry. Unfortunately, a variety of mounting standoff lengths exist; ACCES offers stand-off kits in both 2mm and 2.5mm sizes.

The mPCIe standard, like its PCI Mini Card predecessor, was designed assuming use primarily in Laptop or Notebook and similar devices, where physical dimension is often the paramount design constraint. In Data Acquisition and Control applications low-weight and vibration tolerance tend to be of more concern.

Chapter 6: I/O Interface

Most customers will use the optional cable assembly CAB-mPCIe-ADIO's D-Sub Miniature 37-pin Male connector.



For Singled-Ended analog inputs connect GND to ADC COMMON.

Fully differential input signals must have a path to COMMON for the bias currents of both inputs. Without this path the inputs will float to either rail and exceed the input common mode range of the ADC resulting in a saturated input stage.

A Note About Unused Analog Inputs:

Any unused analog input should be connected to ground with a short wire; either in the mating connector cable, or on the breakout terminal board. This will reduce / eliminate crosstalk which, if left unchecked, can influence measurements of adjacent *connected* input channels.

CAB-mPCIe-ADIO Male 37-Pin Pinout			
S.E. Signal (Diff)	Pin		Assignment
GND	1	20	GND
ADC COMMON	2	21	ADC Ch 0 (Ch 0+)
ADC Ch 1 (Ch 0-)	3	22	ADC Ch 2 (Ch 2+)
ADC Ch 3 (Ch 2-)	4	23	ADC Ch 4 (Ch 4+)
ADC Ch 5 (Ch 4-)	5	24	ADC Ch 6 (Ch 6+)
ADC Ch 7 (Ch 6-)	6	25	GND
GND	7	26	DAC 0
DAC 1	8	27	GND
GND	9	28	GND
Digital GND	10	29	VCCio[1]
Digital GND	11	30	DIO 2
DIO 0 (PWM 0 In)	12	31	Digital GND
GND	13	32	GND
GND	14	33	DAC 2
GND	15	34	DIO 3
DIO 1 (PWM 1 In)	16	35	Digital GND
GND	17	36	GND
GND	18	37	DAC 3
Digital GND	19		

[1]: VCCio pin outputs fused 3.3VDC @ 0.5A on standard models. **-VCCIO** option converts VCCio into a user input between 1.65VDC and 5.5VDC.

For customers needing deeper integration: the on-card connector is a 40-pin latching Molex 501190-4017 connector; the mating connector is the Molex 501189-4010.

40-Pin latching wire-to-board connector			
S.E. Signal (Diff)	Pin		Assignment
ADC Ch 0 (Ch 0+)	1	2	ADC Ch 4 (Ch 4+)
ADC Ch 1 (Ch 0-)	3	4	ADC Ch 5 (Ch 4-)
GND	5	6	GND
ADC Ch 2 (Ch 2+)	7	8	ADC Ch 6 (Ch 6+)
ADC Ch 3 (Ch 2-)	9	10	ADC Ch 7 (Ch 6-)
GND	11	12	GND
COMMON	13	14	GND
GND	15	16	GND*
DAC 0+	17	18	DAC 1+
GND	19	20	GND
GND*	21	22	GND*
VCCio[1]	23	24	GND
DAC 2+	25	26	DAC 3+
GND	27	28	GND
GND	29	30	GND
GND	31	32	GND
Digital GND	33	34	Digital GND
DIO 0 (PWM 0 In)	35	36	DIO 1 (PWM 1 In)
DIO 2	37	38	DIO 3
Digital GND	39	40	Digital GND

*=These pins are not connected to the DB37 connector in our CAB-mPCIe-ADIO cable.

Alternately, custom hardware cables and/or interfaces can be produced to fit your specific application requirement.

Chapter 7: Software Interface

How to use

The ADAS3022 is a flexible data acquisition system-on-chip that has numerous features and modes of operation, and additional modes and features are added by our advanced FPGA design.

This flexibility can seem overwhelming, but we've designed our AIOAIO.dll API to make using this ADC simple for 99% of customer use-cases, based on 30+ years of customer feedback.

We strongly recommend you ignore the register details provided in Chapter 7: Software Interface and the discussions regarding low-level control of the ADC in the second half of this chapter. Instead, simply refer to the AIOAIO Software Reference (.html) manual [link] and the source code to the variety of sample programs provided in the Software Installation Package [link].

Tip: Taking data from every channel can be as simple as calling "ADC_GetImmediateScanV(0, rangeCode, &data);", which converts all channels at the specified range and stuffs the data (as double-precision floating point Voltages) into the data array. This function can be called many thousands of times per second. Please refer to the samples and the software reference for details on this and other available API functions, including how to acquire 1MHz data via callback or polling.

Advanced Topics

BASIC, ADVANCED, AND NON-SEQUENCED MODES

The ADAS3022 uses the SEQ1:0 bits in the +38 control register to select between non-sequenced mode, basic sequence mode, and advanced sequence mode.

SEQ1	SEQ0	Mode	Description
0	0	non-Sequenced	The ADAS will acquire data from the channel specified in the INx2:0 bits, at the gain specified in the Gain2:0 bits.
0	1	Modify Basic Sequence	Allows the gain and such to be modified while running a basic sequence, without starting conversions over at CH0.
1	0	Advanced Sequence	Acquires Channel 0 using the gain selected via +18 bits 2:0. Conversion-starts will automatically cycle through the channels from CH0 through INx2:0, and each channel is acquired at the per-channel gain set in +18. The sequence repeats, starting at CH0 after INx2:0 is acquired.
1	1	Basic Sequence	Acquires channel 0 using the gain set in Gain2:0. Conversion-starts will automatically cycle through the channels from CH0 through INx2:0, but all channels are acquired using the gain set in Gain2:0 rather than using the gains from +18. The sequence repeats, starting at CH0 after INx2:0 is acquired.

SOFTWARE, PERIODIC, AND EXTERNAL START ADC CONVERSION TIMING MODES

ADC data can be acquired periodically, synchronous to an external digital input, or asynchronously via software command.

Single, Asynchronous: If the +10 ADC Timing divisor is zero then writing to +38 with bit 16 set (to 1) will initiate a single ADC Start Event under software control.

Periodic, Asynchronous: If the +10 ADC Timing divisor is non-zero, and the External ADC Trigger Digital Input Secondary function is *not* enabled, writing to +38 with bit 16 set will initiate a single ADC Start Event, and subsequent events will occur at the rate selected via +10's divisor. This is "software initiated periodic timed ADC" data.

External Trigger, Periodic, Synchronous: If the +10 ADC Timing divisor is non-zero, and the External ADC Trigger Digital Input Secondary function is enabled, writing to +38 with bit 16 set ARMS the card to begin the periodic collection of ADC data. No data will be collected until the selected edge occurs on the ADC Trigger input. (Refer to +48 for additional details on the Digital I/O Secondary Functions.) Once triggered, data will be collected until manually stopped by writing +38 with bit 16 clear (or various resets, etc.).

External Start, Single, Synchronous: Enable enSTART at +48 bit 18 and select the active edge with bit 19. Each selected edge on DIO2 initiates an ADC Start Event. With SCAN set, each event acquires the configured scan; otherwise it acquires one conversion.

SINGLE AND SCAN START MODES

Each ADC Start Event can be configured to start either a Scan of channels or a single channel conversion.

Single Start Mode: Writing to +38 with bit 18 clear (to 0) selects "Single Start Mode". Each ADC Start Event, regardless of source, will acquire one channel. No subsequent conversions will occur until the next ADC Start Event.

Scan Start Mode: Writing to +38 with bit 18 set (to 1) selects "Scan Start Mode". Each ADC Start Event will acquire the full configured sequence of channels, starting with CH0 and proceeding through INx2:0, then no further data will be acquired until a subsequent ADC Start Event. The channels within this "scan" of data are acquired at the rate selected via +14. Bit 18 is ignored (assumed zero) if non-Sequenced mode is set (SEQ1:0=00) or if INx2:0==0.

Software Pro Tips:

- Use our API. Avoid accessing the card registers unless you really know you need to. Contact us for any questions, we're here to help.
- Always use Advanced Sequencer Mode.
- Always use Scan Start Mode.
- Set the periodic rate at +10, set the inside-scan channel rate at +14, configure External Trigger if you are using it, configure the per-channel gains at +18, then write to +38 to Start or Arm (in Software or ADC Trigger modes, respectively) the Periodic Scans.

Register Overview

Register Offset [hex]	Read /Write	Register Name	Register Description Note: All registers must be accessed as 32-bits
+0	R/W	Resets and Power	Board and Feature Reset command bits and ADC Power-Down control bit and status
+4	W	DAC Control	DAC (LTC2664) Command Register bits
+8*	W	DAC Waveform Divisor	DAC Waveform Points/second divisor = Base Clock / DAC Waveform Rate (this register)
+C	R	ADC Base Clock	Frequency of the ADC Sequencer Base Clock (Hz) used to calculate the ADC Rate Divisor for desired conversion rates
+10	W/R	ADC Rate Divisor	ADC Start Rate = ADC Base Clock / ADC Rate Divisor (this register)
+14	W/R	ADC Rate Divisor #2	Controls rate of channels inside each scan when running in scan-start mode
+18	W/R	ADC ADV Sequence Gain	Each nybble controls the gain code (input range) of the respective ADC channel
+20	W/R	ADC FAF Threshold	ADC FIFO Almost Full Threshold, can be enabled to generate IRQs when the threshold amount of ADC data is available in the FIFO
+28	R	ADC FIFO Count	ADC FIFO Depth: read to determine how much data is available in the FIFO
+30	R	ADC FIFO Data	ADC FIFO
+38	W/R	ADC Control	ADAS3022 and ADC Control bits
+40	W/R	IRQ Enable / Status	IRQ Latch Clear bits and IRQ Enable Control bits ÷ IRQ Latch Status and IRQ Enable Status
+44	W/R	DIO Data	4-bits of DIO Data. Must be read/written as a 32-bit DWORD value
+48	W/R	DIO Control	Digital Secondary Function enable, edge, and direction control bits for a total of four I/O Groups (DIO 3:0)
+4C	W/R	Watchdog Timer	Watchdog Timer Control
+50*	RW	DAC Waveform FIFO	Write DAC Control values here to load into the DAC Waveform FIFO; read to determine how many samples are in the FIFO
+54*	W	DAC Waveform DACs/Point	Write 1, 2, 3, or 4 to configure how many samples are written from the DAC Waveform FIFO to the DACs on each DAC Waveform tick
+58*	R	DAC Waveform FIFO Size	Size of the DAC Waveform FIFO (+50) in number of 32-bit DAC control values (0x2000 is typical)

Register Offset [hex]	Read /Write	Register Name	Register Description Note: All registers must be accessed as 32-bits
+60*	RW	ADC CH0 HIGH Threshold	16-bit value above which ADC CH 0 reading can generate an IRQ/status
+64*	RW	ADC CH0 LOW Threshold	16-bit value below which ADC CH 0 reading can generate an IRQ/status
+68	R	FPGA Rev Code	FPGA Rev Code
+6C	R	DeviceID	Bits 15:0 identify the detected model
+C0/+C4**	RW	ADC Calibration Gain 0	32-bit floating-point scale / offset for this gain code
+C8/+CC**	RW	ADC Calibration Gain 1	32-bit floating-point scale / offset for this gain code
+D0/+D4**	RW	ADC Calibration Gain 2	32-bit floating-point scale / offset for this gain code
+D8/+DC**	RW	ADC Calibration Gain 3	32-bit floating-point scale / offset for this gain code
+E0/+E4**	RW	ADC Calibration Gain 4	32-bit floating-point scale / offset for this gain code
+E8/+EC**	RW	ADC Calibration Gain 5	32-bit floating-point scale / offset for this gain code
+F0/+F4	—	Reserved	Gain code 6 is reserved; do not access
+F8/+FC**	RW	ADC Calibration Gain 7	32-bit floating-point scale / offset for this gain code
+120**	R	PWM 0 Low Pulse Width	32-bit register reads the most recent low-going pulse duration on DIO # 0
+124**	R	PWM 0 High Pulse Width	32-bit register reads the most recent high-going pulse duration on DIO # 0
+220**	R	PWM 1 Low Pulse Width	32-bit register reads the most recent low-going pulse duration on DIO # 1
+224**	R	PWM 1 High Pulse Width	32-bit register reads the most recent high-going pulse duration on DIO # 1

Note *: These registers are only functional on the FDS models. **: Calibration and PWM input registers are only functional on 16-bit F and FDS models.

All of these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AIOWDM [for Windows], APCI [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes. Addresses not explicitly documented are factory reserved and should not be accessed.

REGISTER DETAILS

Register bits labeled UNUSED or RSV are reserved and should be cleared to zero in all write operations and ignored in all read operations.

Resets and Power, Offset +0 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map								
bit	D31 THROUGH D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	RST FIFO	RST DIO	UNUSED	RST DAC	PD ADC	RST ADC	RST BOARD

RST FIFO: Writing with bit D6 set will reset the ADC FIFO, returning it to the power-on / reset state: emptying the FIFO by throwing away the contents.

RST DIO: Writing with bit D5 set will reset the Digital I/O circuits to their power-on / reset state: returning all I/O Groups to input mode and disabling secondary functions.

RST DAC: Writing with bit D3 set will reset the Analog Output circuits to their power-on / reset state: ±10V range on all DAC outputs with 0V on each output.

PD ADC: Writing a 1 will power the ADAS3022 down. Write a 0 to power the ADAS3022 back up. Only this bit does not auto-clear to zero on write.

RST ADC: Writing a 1 will reset the Analog Input circuits to their power-on / reset state: see each ADC Register for more details

RST BOARD: Writing a 1 will reset the entire device, including the DMA engine, to its power-on / reset state.

All RST bits are “command” bits: a 1 causes the reset to occur, and the reset clears the 1.

DAC Control, Offset +4 of 32-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

bit	D31	D30	D29	D28	D27-D24	D23 through D20				D19 through D16				D15 through D0
Name	DAC SPI busy	LDAC	DAC FIFO Empty	DAC FHE	unused	C3	C2	C1	C0	A3	A2	A1	A0	16-bit DAC Counts (0-FFFF)

Bits 31, 30, 29, and 28 are read-only. Bits 29 and 28 only exist on the FDS models.

Bit 31: If set the DAC SPI bus is busy; avoid writing to +4 while this bit is set

Bit 30: If set the DAC has been loaded since the last time +4 was read (clears on read)

Bit 29: If set the DAC Waveform FIFO is empty

Bit 28: If set the DAC Waveform FIFO is less than half full

Please refer to the LTC2664 Data Sheet for details regarding bits D23-D0

Consult the AIOAIO Software Reference, or our sample programs' source, to avoid the hassle:

DAC_SetRange1(iBoard, iChannel, iRange);

DAC_OutputV(iBoard, iChannel, double Voltage);

DAC Waveform Rate Divisor, Offset +8 of 32-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

Write a 32-bit divisor to control the speed at which DAC Waveform playback occurs (Points per second). Each timeout of this clock causes the DACs to simultaneously output the last loaded values; the FPGA then writes the next Point from the DAC Waveform FIFO to the DAC chip. A Point consists of 1, 2, 3, or 4 DAC control words as specified at +54.

DAC Waveform Rate Divisor = integer(Base Clock ÷ Target DAC Waveform Output Rate)

Actual DAC Waveform playback (Points/second) Rate (Hz) = Base Clock ÷ DAC Waveform Rate Divisor

FDS models only

Base Clock, Offset +C of 32-bit Memory BAR[1] Read Only 32-bits only Back to Register Map

Base Clock: Reading this 32-bit register returns the speed (in Hertz) of the clock used to generate ADC Start Conversions. Typical value is 50Million (50MHz), but for broadest compatibility software should always read this register during init, and always use the read value when calculating what, if any, divisors to write to the ADC Rate Divisor, DAC Waveform Rate Divisor, and Watchdog timeout registers.

ADC Base Clock, Offset +C of 64-bit Memory BAR[1] Read Only 32-bits only Back to Register Map

ADC Base Clock: Reading this 32-bit register returns the speed (in Hertz) of the clock used to generate ADC Start Conversions. Typical value is 50 Million (50MHz), but for broadest compatibility software should always read this register during init, and always use the read value when calculating what, if any, divisor to write to the ADC Rate Divisor register.

ADC Rate Divisor, Offset +10 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

ADC Rate Divisor: Write a 32-bit divisor to the ADC Rate Divisor register to control the speed at which ADC Start events occur.

Actual ADC Start Rate (Hz) = ADC Base Clock ÷ ADC Rate Divisor

ADC Rate Divisor = integer(ADC Base Clock ÷ Target ADC Start Rate)

In ADC Scan Start mode each timeout of the +10 divisor begins a scan of channels. In all other modes the +10 rate selects the conversion rate per-channel.

ADC Rate Divisor #2, Offset +14 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

ADC Rate Divisor #2: Write a 32-bit divisor to the ADC Rate Divisor #2 register to control the speed at which ADC Conversions occur within each scan when running in ADC Scan Start Modes.

In "ADC Scan, Timer Start" modes only, one Scan of ADC CH0 through the channel selected in +38 INx2:0 bits occurs at the rate selected at +10. In all "Scan Start modes" during each Scan the first channel is converted immediately at ADC Start, and subsequent channels are acquired at the rate selected at +14.

ADC Advanced Sequencer Gain Control, Offset +18 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map																														
bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSV	AIN 7 GAIN2:0			RSV	AIN 6 GAIN2:0			RSV	AIN 5 GAIN2:0			RSV	AIN 4 GAIN2:0			RSV	AIN 3 GAIN2:0			RSV	AIN 2 GAIN2:0			RSV	AIN 1 GAIN2:0			RSV	AIN 0 GAIN2:0		

Each nybble configures the gain of the corresponding Analog Input channel ONLY when the ADC is running in Advanced Sequenced mode.

Table 1 - Gain Codes

GAIN2:0 "gain code"	D2	D1	D0	Range Volts *per pin*[1]	Range V p-p, MAX[1]	µV/Count	Differential rejection V	Notes
0	0	0	0	*Reserved*				The voltage range is shown as recommended max voltage per input pin. The recommendation is slightly narrower than max to allow calibration. The voltages that can be *measured,* between the + input and the – or COMMON inputs, are double: the ±12V range will return voltages between +24V and -24V, or "48V p-p".
1	0	0	1	±5	20.48	312.5	±5.12	
2	0	1	0	±2.5	10.24	156.3	±7.68	
3	0	1	1	±1.25	5.12	75.13	±8.96	
4	1	0	0	±0.625	2.56	39.06	±9.60	
5	1	0	1	±0.3125	1.28	19.53	±9.92	
7	1	1	1	*Reserved*				

Gain code 6 (110) is reserved and will result in undefined behavior

Note 1: Applying +V to IN+ and -V to IN- (or ADC COMMON) results in 2×V span; reversing the voltage polarity results in another 2×V span, for a total Peak-to-Peak measurement capability of 4×V p-p

ADC FIFO Almost Full IRQ Threshold, Offset +20 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map		
bit	D31 through D12	D10 through D0
Name	UNUSED	FAF

FAF: Write any 12-bit value (0..2047) to set the amount of entries in the ADC FIFO allowed to accumulate before a FIFO Almost Full IRQ is fired.
In Software ADC Start mode (ADC Rate Divisor (+10) cleared to zero) the FIFO is 32-bits wide, able to hold up to 2047 conversion results (+statuses).

ADC FIFO Count, Offset +28 of 64-bit Memory BAR[1] Read-Only 32-bits only Back to Register Map		
bit	D31 through D12	D10 through D0
Name	UNUSED	FIFO Count

FIFO Count: Read FIFO Count to determine how many entries the ADC FIFO contains.
The FIFO Count determines how many ADC Conversions (+statuses) are held in the FIFO. Read the ADC FIFO this many times to gather the acquired ADC Data.

ADC FIFO Data, Offset +30 of 64-bit Memory BAR[1] Read-Only 32-bits only Back to Register Map													
bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22 through D20	D19	D18 through D16	D15 through D0
Name	INVALID	RUNNING	DIO3	DIO2	DIO1	DIO0	TEMP	MUX	RSV	Channel	Diff	Gain	ADC Counts (Two's complement)

ADC FIFO Data: Read the RAW-format ADC Conversion results (in twos-complement 16-bit form) and the associated status word.

INVALID: If INVALID is SET then all other bits are undefined and the entry should be discarded. This can occur if you read from the ADC FIFO while the ADC FIFO Count (+28) is zero.

DMA data: In software-immediate and external ADC Start modes, the upper 32-bit entry of a DMA read is marked INVALID. Check the INVALID bit of each ADC data entry and discard entries with this bit set.

RUNNING: SET indicates the ADC Sequencer is operating, taking either periodic (timer-driven) conversions or via the external ADC Start secondary digital function.

DIO3:0: These four bits indicate the state of the corresponding digital I/O pin at the time the paired ADC Conversion was sampled.

TEMP: If TEMP is CLEAR the ADC Counts are acquired from the ADAS3022's onboard temperature sensor rather than from an analog input channel. Refer to ADC Control (+38) for more information about acquiring the temperature data.

MUX: If MUX is CLEAR the ADC Counts are acquired from the ADAS3022's Auxiliary Mux inputs rather than from the normal Analog Input Channels. Note, the mPCIe-ADIOHC16-8F does not have anything usefully connected to the Aux Mux inputs and you should not bother acquiring data from them.

Channel2:0: The 3 Channel bits indicate from which Analog Input the paired ADC Counts were sampled. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Diff: SET indicates the paired ADC Counts were sampled in Differential mode. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Gain2:0: The 3 Gain bits indicate at what gain code the paired ADC Counts were sampled. Refer to the gain code table in ADC Advanced Sequencer Gain Control (+18) for how to interpret the Gain bits.

ADC Counts: 16-bit two's complement ADC counts, the ADC conversion result from the samples Channel at the specified Gain, sampled in Differential or Singled-ended / Pseudo-Differential mode as indicated by the Diff bit (D19).

Please refer to the sample program's source for details on how to translate RAW-format ADC data into Volts — or skip the hassle and use our AIOAIO.dll API Library:

ADC_GetImmediateV(iBoard, pVolts, iChannel, iRange);, ADC_GetImmediateScanV(iBoard, pVolts[]); etc.

ADC Control, Offset +38 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map															
bit	D31 through D19	D18	D17	D16	D15	D14 through D12	D11	D10	D9 through D7	D6	D5 through D4	D3	D2	D1	D0
Name	UNUSED	SCAN	CONFIG	GO	RSV	INx2:0	COM	RSV	Gain2:0	/MUX	SEQ1:0	/TEMP	RSV	CMS	RSV

The ADAS3022 is a very flexible ADC module and we highly recommend you use the AIOAIO.dll-provided API to avoid needing to know the following information.

SCAN: If SCAN is set (to 1) *AND* INx2:0 is non-zero then each "ADC Start" event will acquire channels 0 through INx2:0 at the rate specified in +14.

CONFIG: If CONFIG is set then the ADC control bits (D15 through D0 of this register) will be written to the ADAS3022

GO: If GO is set then, if +10 is non-zero the card will begin taking ADC conversions or scans at the rate set via +10; if +10 is zero then a single ADC conversion or scan will be taken.

INx2:0: INx specifies the individual channel to convert (in non-sequenced modes) or the last channel of the 0-INx sequence to be converted.

COM: If COM is set then each conversion will be the measurement between the IN+ pin and COMMON (single-ended or pseudo-differential mode). If COM is clear then differential mode is set, and each conversion will be the measurement between the IN+ and IN- pins.

Gain2:0: If BASIC or non-sequenced mode is configured via the SEQ1:0 bits then Gain2:0 selects the gain to be used for the conversion(s) commanded. If advanced sequence mode is configured then these bits are ignored (bits 2:0 at +18 take precedence in advanced sequencer mode)

/MUX: All users should set this bit to "1" unless otherwise instructed by the factory. If MUX is clear (0) then the conversion will be from the auxiliary mux inputs (in non-sequencer mode) or the sequence will include the aux input (sequencer modes). Not recommended.

SEQ1:0: Use "00" for non-sequenced mode and "10" for advanced sequencer mode. "11" sets basic sequencer mode, and "01" updates the basic sequence-in-progress. Not recommended.

/TEMP: If TEMP is clear (0) then the conversion will be from the onboard temperature reference (in non-sequencer mode) or the sequence will include the temperature input (sequencer modes). Not recommended. Most users should set this bit to 1.

CMS: Must be set if conversion will occur slower than 1kHz. Must be clear if conversions will occur faster than 900kHz.

IRQ Enable/Clear and Status, Offset +40 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	WDG	UNUSED	UNUSED	ADCLO	ADCHI	DACEMPTY	DACHF	UNUSED	EXT	LDAC	FOF	FAF	DTO	DDONE	ADCSTART	ADCTRIG

bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	UNUSED	UNUSED	enADCLO	enADCHI	enDACEMPTY	enDACHF	UNUSED	enEXT	enLDAC	enFOF	enFAF	enDTO	enDDON	enADCSTART	enADCTRIG

Read IRQ Status to determine which IRQs have fired (D28 through D16), if the Watchdog has Barked (D31), and which IRQs are enabled (D12 through D0). Reserved bits are ignored.

WDG: If WDG is SET then the Watchdog Timer has Barked (timed out). Refer to Watchdog Control (+4C) for details on using the Watchdog Timer feature.

ADCLO: If ADCLO is SET the value on ADC CH 0 is below the value set at the +64 register

ADCHI: If ADCHI is SET the value on ADC CH 0 is above the value set at the +60 register

DACEMPTY (D26): SET when the DAC Waveform FIFO is completely drained. Set enDACEMPTY (D10) to enable this IRQ. FDS models only.

DACHF (D25): SET when the DAC Waveform FIFO reaches its half-full threshold while draining (4096 command values). Set enDACHF (D9) to enable this IRQ. FDS models only.

EXT: If EXT is SET then an IRQ has been fired from the DIO1 Secondary Function “External IRQ”. Refer to DIO Control (+48) for details on DIO Secondary Functions.

LDAC: If LDAC is SET then an IRQ has been fired from the DIO0 Secondary Function “LDAC”. Refer to DIO Control (+48) for details on DIO Secondary Functions.

FOF: If FOF is SET then an IRQ has been fired because the ADC FIFO has Overrun: More data was acquired than fit in the ADC FIFO.

FAF: If FAF is SET then an IRQ has been fired because the ADC FIFO Count (+28) has reached the configured FIFO Almost Full IRQ Threshold (+20).

DTO: If DTO is SET then a DMA Timeout IRQ has been fired.

DDONE: If DDONE is SET then a DMA Done IRQ has been fired.

ADCSTART: If ADCSTART is SET then an IRQ has been fired from the DIO2 Secondary Function “ADCSTART”. Refer to DIO Control (+48) for details on DIO Secondary Functions.

ADCTRIG: If ADCTRIG is SET then an IRQ has been fired from the DIO3 Secondary Function “ADCTRIG”. Refer to DIO Control (+48) for details on DIO Secondary Functions.

Bits D12 through D0 indicate if the corresponding IRQ has been enabled.

Write IRQ Status bits SET to clear the latched IRQ Status bit(s). Typically, code will read +40 and write the value to +40 to clear all detected IRQs and leave the IRQ enables unchanged.

Write IRQ Enable bits SET to enable corresponding IRQ sources.

DIO Data, Offset +44 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

bit	D31 through D4	D3	D2	D1	D0
Name	UNUSED	DIO3	DIO2	DIO1	DIO0
I/O GROUP		3	2	1	0

Read DIO Data to read the digital input pins or to readback the last commanded digital output state.

Write to DIO Data to configure the digital pin(s)’ high/low state for those bits in I/O Groups configured as Outputs. SET bits will output high voltage, CLEAR bits will output GND.

Refer to DIO Control (+48) for how to configure the input vs output direction of each I/O Group.

DIO Control, Offset +48 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map																			
bit	D31, D30	D29	D28	D27	D26	D25, D24	D23	D22	D21	D20	D19	D18	D17	D16	D15:D4	D3	D2	D1	D0
Name	unused	enDAC_SYNC	edgeFDS_TRIG	enFDS_TRIG	enWDT	unused	edgeEXT	enEXT	edgeLDAC	enLDAC	edgeSTART	enSTART	edgeTRIG	TRIG	unused	IOG3	IOG2	IOG1	IOG0

Write DIO Control to enable Digital Secondary Functions, and to control the input vs output direction of each Digital I/O Group.

enDAC_SYNC (D29): SET to output the DAC Waveform timer clock on DIO0 as 40ns high-going pulses at the rate selected by +8. DIO0 becomes an output. CLEAR to disable this clock output. FDS models only.

enFDS_TRIG (D27): SET to start Fast DAC Streaming Waveform playback on the selected trigger edge at DIO0. DIO0 becomes an input. This function takes precedence over enLDAC; configure the DAC rate at +8 and load the FIFO before triggering. Further edges are ignored while playback is running. After the FIFO empties, loading new waveform data rearms the next trigger. FDS models only.

edgeFDS_TRIG (D28): SET to select a rising edge, CLEAR for a falling edge. Preserve the other +48 function and direction bits when changing the trigger configuration.

enWDT: SET enWDT to enable the "WDT Output Status" Digital Output Secondary Function on DIO1. DIO1 (I/O Group 1) becomes an output and indicates the state of the Watchdog Feature.

enEXT: SET enEXT to enable the "External IRQ" Digital Input Secondary Function on DIO1 so the selected edge on the input will (optionally) generate IRQs.

enLDAC: SET enLDAC to enable the "External LDAC" Digital Input Secondary Function on DIO0 so the selected edge will cause the DACs to update and optionally generate an IRQ.

enSTART: SET enSTART to enable the "ADC Start Conversion" Digital Input Secondary Function on DIO2 so the selected edge will cause an ADC Start Event and optionally generate an IRQ.

enTRIG: SET enTRIG to enable the "ADC Trigger" Digital Input Secondary Function on DIO3 so the selected edge will trigger timed ADC conversions and optionally generate an IRQ. Consult the "Software Tips" section for details on using ADC Trigger.

Each Digital Input Secondary function has a configurable active edge, rising or falling. SET the corresponding edge*XXX* bit to select rising edge, CLEAR the bit for falling edge.

IOG*x*: SET each IOGx bit to configure the digital I/O bit in the associated I/O Group for use as a digital output. CLEAR an IOG*x* bit to configure the I/O Group for use as input.

Watchdog Control, Offset +4C of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map																															
bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Watchdog Timeout																															

Write the number of Ticks (which occur at the ADC Base Clock Rate (+C)) before the Watchdog should timeout ("Bark"); e.g. for a one-second timeout period write the value read from +C to +4C.

When the Watchdog Barks the board is RESET as if just powered on (or as if a 1 is written to the Resets and Power (+0) register) with the following exceptions:

If the "WDT Output Status" DIO Secondary Function is enabled then DIO1 remains an output and asserts 0.

Bit D31 of the IRQ Enable/Clear and Status (+40) "WDG" is latched SET to indicate that the Watchdog timed out.

Write 0 to the Watchdog Timeout (+4C) register to disable the Watchdog Feature.

DAC Waveform FIFO, Offset +50 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

DAC Waveform FIFO: Write DAC commands to load the DAC Waveform FIFO. Generally 0x000nCCCC where n is the DAC# and CCCC is the counts. Read returns the number of control values currently in the FIFO.

FDS models only

DAC Waveform DACs/Point, Offset +54 of 64-bit Memory BAR[1] Read/Write 32-bits only Back to Register Map

DAC Waveform DACs/Point: Write 1, 2, 3 or 4 to specify how many DACs are being used for Waveform Playback.
FDS models only

DAC Waveform FIFO Size, Offset +58 of 64-bit Memory BAR[1] Read 32-bits only Back to Register Map

DAC Waveform FIFO Size: Read to determine the DAC Waveform FIFO size in 32-bit DAC command values. Typically 0x2000, or 8192 values.
FDS models only

ADC CH0 High Threshold, Offset +60 Read/Write 32-bits only Back to Register Map

Write a 16-bit two's-complement ADC count threshold in bits 15:0. The reset value is 0x00007FFF. When an acquired ADC CH0 value exceeds this threshold, ADCHI (+40 bit 27) is set. Set enADCHI (+40 bit 11) to enable its IRQ. FDS models only.

ADC CH0 Low Threshold, Offset +64 Read/Write 32-bits only Back to Register Map

Write a 16-bit two's-complement ADC count threshold in bits 15:0. The reset value is 0x00008000. When an acquired ADC CH0 value falls below this threshold, ADCLO (+40 bit 28) is set. Set enADCLO (+40 bit 12) to enable its IRQ. FDS models only.
Thresholds use ADC counts, not volts. Select threshold counts for the gain code used to acquire CH0. These comparisons operate on acquired data; they do not start ADC conversions.

FPGA Rev Code, Offset +68 Read Only 32-bits only Back to Register Map

Read this register to obtain the FPGA Rev Code. Include this value when requesting technical support.

DeviceID, Offset +6C Read Only 32-bits only Back to Register Map

Bits 15:0 return the DeviceID of the detected model. Refer to the model table in Chapter 3 for the corresponding DeviceID values.

ADC Calibration, Offsets +C0 through +FC Read/Write 32-bits only Back to Register Map

16-bit F and FDS models provide a separate calibration scale and offset for each supported ADC gain code. Each register contains a 32-bit IEEE-754 floating-point value, written as its raw 32-bit representation. The selected gain code determines which scale/offset pair is applied to acquired ADC data.

Reset defaults are scale 1.0 (0x3F800000) and offset 0.0 (0x00000000). These defaults leave the ADC data unadjusted. Gain code 6 and offsets +F0/+F4 are reserved. The register addresses below do not make a reserved input range available; use only the gain codes supported by the model.

Gain code	Scale register	Offset register
0	+C0	+C4
1	+C8	+CC
2	+D0	+D4
3	+D8	+DC
4	+E0	+E4
5	+E8	+EC
7	+F8	+FC

Use the gain-code definitions in ADC Advanced Sequencer Gain Control (+18) to select the matching calibration pair. Program calibration values before starting acquisition.

PWM Input Pulse Widths, Offsets +120, +124, +220, +224 Read Only 32-bits only Back to Register Map

16-bit F and FDS models measure the high and low pulse durations on DIO0 and DIO1. Configure the measured line as an input with its IOG bit at +48 cleared; disable secondary functions that drive that line as an output.

DIO0: +120 returns the most recent low-pulse duration; +124 returns the most recent high-pulse duration. DIO1: +220 returns the most recent low-pulse duration; +224 returns the most recent high-pulse duration. Each register is a 32-bit measured count.

Each count represents 8ns. Pulse duration = count × 8ns. For nonzero (low count + high count), frequency in Hz = 125000000 ÷ (low count + high count), and high-state duty cycle (%) = 100 × high count ÷ (low count + high count).

DIO0 is pin 12 and DIO1 is pin 16 on the DB37 cable connector (pins 35 and 36, respectively, on the on-card 40-pin connector).

PCI Express Mini Card Plug-and-Play Data	
BAR[n]	Description
0	DMA Registers
1	I/O Registers

In Windows[1], please consult the various samples (C#, Delphi, and more) to explore how to program the device. The AIOAIO Software Reference Manual.pdf provides reference material covering all AIOAIO Library APIs.

Under certain circumstances the following information might prove useful:

A NOTE ABOUT PERFORMANCE

The PCI Express bus and the PCI Express Mini Card standard are capable of very high bandwidth, but the latency per-transaction is roughly the same as all the other busses – it hasn't improved in decades. This means you can expect to usually see a not-less-than 1MHz transaction rate. Typical rates exceed 3MHz [0.3µs].

Unfortunately, modern Operating Systems have introduced a new source of latency, the kernel / userland division. Application code runs in userland, which must transition to the kernel in order to perform any hardware operation. This transition adds quite a lot of latency, which varies between different OSes, motherboards and revisions thereof, etcetera. A Windows XP system can see an additional 7µs per transaction; a modern computer might see 3µs or less. Any transaction from the kernel itself, however, avoids this additional overhead.

Real-time operating systems will enable the highest transaction rates possible, all the way up to the hardware limits.

[1] *In Linux or OSX please refer to the documentation at* github.com/accesio/apci.

The latest information can always be found on the product page on the website. Here are some useful links:

Links to useful downloads	
ACCES web site	https://accesio.com
Product web page	accesio.com/product/mPCIe-ADIOHC16-8FDS
This manual	accesio.com/MANUALS/mPCIe-ADIOHC16-8FDS.pdf
Install Package	accesio.com/files/packages/M.2-_mPCIe-ADIOHC16-8F Install.exe
Linux / OSX	github.com/accesio/APCI

Chapter 8: Specifications

PC Interface

PCI Express Mini Card	Type F1 "Full Length"

Analog Inputs

ADC Type	Successive approximation
Resolution	16-bit differential bipolar ADC
Sampling rate	1 MSPS
Number of channels	8 Single-ended or 4 Differential (software selectable)
Differential Bipolar Ranges (V)	±5, ±2.5, ±1.25, ±0.625, ±0.3125V
4-20mA or 10-50mA	Factory options
Int Nonlinearity Error	±0.6 LSB to ±1.5LSB, varies with gain
No Missing Codes	16 bits
Input Impedance	> 500MΩ
A/D Start Sources	Software Start, Timer Start, External Start, Externally Triggered Timer Start
A/D Start Types	Single Channel or Scan
Overvoltage Protection	Current limiting through 2 KΩ
Crosstalk	-120dB @ 10kHz

Analog Outputs

Number	4
Type:	Single-Ended
Resolution:	16-bit
Output Ranges:	±2.5, 0-5V, ±5V
Settling Time	9.5us typical, ±5V (±1LSB at 16 bits)
Output Current	max ±18 mA per channel

Digital Input / Output Interface

Digital Bits		4
Performance		1 µs per transaction max (~3.5µs in non-kernel Windows)
Digital Inputs (Standard Version)	Logic High Logic Low	2.0V to VCCIO (3.3VDC, 5VDC tolerant) 0V to 0.8V
Digital Outputs (Standard Version)	Logic High Logic Low Power Output	2.4V (min) 24 mA source 0.55V (max) 24 mA sink +3.3 VDC via 0.5A polyfuse (resetting)
Digital Inputs w/user VCCIO (-VCCIO Option)	SN74LVC1T45DRLR Logic High Logic Low	Buffer chip bits 0-3 (individual direction) 3.5V to 5V, UVCCIO = 5V 0V to 1.5V, UVCCIO = 5V
Digital Outputs w/user VCCIO (-VCCIO Option)	1.65V to 5.5V Logic High Logic Low	At DB37M, via polyfuse 3.8V (min) 32mA UVCCIO = 4.5V 0.55V (max) 32mA UVCCIO = 4.5V
Termination	10 K Ohm pullups (pulldowns and no-bias optional)	

Environmental

Temperature	Operating	0°C to +70°C -40°C to +85°C (-T option)
	Storage	-40°C to +105°C
Humidity		5% to 95% RH, non-condensing
Dimensions, mPCIe	Length	50.95mm (2.006")
	Width	30.00mm (1.181")
Weight	mPCIe	6.6 g

Power

Power required, mPCIe	1.5 W

I/O Interface Connectors

On card	Molex 501190-4017 40-pin latching
Mating	Molex 501189-4010
On-cable	Male, D-Sub Miniature, 37-pin
Mating	Female, D-Sub Miniature, 37-pin

Model Options

-T	Extended Temperature Operation (-40° to +85°C)
-I / -ID	4-20mA inputs (Singled-ended / Differential)
-VCCIO	User-supplied digital I/O VCC
-PD	Pull-downs on Digital I/O lines
-Sxx	Special configurations (10-50mA inputs, input voltage dividers, conformal coating, etc.)

Chapter 9: Certifications

CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

UL & TUV

Neither DC voltages above 3.3V, nor AC voltages of any kind, are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

ROHS / LEAD-FREE STATEMENT

All models are produced in compliance with RoHS and various other lead-free initiatives.

WARNING

A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES

equipment not approved in writing by ACCES or, if in ACCES' opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

FIRST THREE YEARS: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

FOLLOWING YEARS: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

DISCLAIMER

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PCI EXPRESS MINI CARD STANDARD NOTICE AND EXCEPTION

The mPCIe-ADIOHC16-8FDS and M.2-ADIOHC16-8FDS families of devices are fully compliant with PCI Express Mini Card v1.2 and M.2 B&M keys, respectively.